REMARKS

After entry of this amendment, claims 1-29 and 31-35 remain pending. In the present Office Action, claims 18-29 were rejected under 35 U.S.C. § 101. Claims 10-17 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-3, 10-12, 18-20, 23-28, and 30 were rejected under 35 U.S.C. 102(b) as being anticipated by Motorola MC68030 Enhanced 32-Bit Microprocessor User's Manual, Second Edition ("Motorola"). Claim 29 was rejected under 35 U.S.C. 103(a) as being unpatentable over Motorola in view of Uffenbeck, Microcomputers and Microprocessors, the 8080, 8085, and Z-80 Programming, Interfacing, and Troubleshooting ("Uffenbeck"). Claims 1-4, 7-13, and 16-30 were rejected under 35 U.S.C. 102(b) as being anticipated by Sites et al., Alpha Architecture Reference Manual ("Sites"). Claims 18-29 were rejected under 35 U.S.C. § 102(a) as being anticipated by Jan Hubicka, email posted to patchs@x86-64.org ("Hubicka"). Applicant respectfully traverses these rejections and requests reconsideration. Claims 5-6 and 14-15 were objected to but would be allowable if rewritten in independent form.

Motorola Rejection

Applicant respectfully submits that each of claims 1-29 recites a combination of features not taught or suggested in Motorola, nor Motorola in view of Uffenbeck. For example, claim 1 recites a combination of features including: "a segment register configured to store a segment base address and a selector which, in at least one operating mode, locates a segment descriptor in a segment descriptor table in memory...wherein the execution core is configured, in response to a first instruction, to swap the segment base address in the segment register and the address in the register".

The present Office Action asserts that Motorola teaches a segment register as the address registers shown in Figure 1-2 on page 1-4 and described in section 2.4.8 on page 2-10. However, it appears that Motorola's address registers store only a memory address (see the figure in section 2.4.8 on page 2-10, in which an address register stores a 32 bit memory address). Thus, Motorola's address register does not teach or suggest "a segment register configured to store a segment base address and a selector which, in at least one

operating mode, locates a segment descriptor in a segment descriptor table in memory" as recited in claim 1.

Furthermore, the Office Action asserts that Motorola teaches the first instruction via the exchange instruction described on page 3-101. However, the exchange instruction either exchanges data registers, exchanges address registers, or exchanges an address register and a data register (see Motorola, page 3-101). This does not teach or suggest "the execution core is configured, in response to a first instruction, to swap the segment base address in the segment register and the address in the register" wherein the segment register is "configured to store a segment base address and a selector which, in at least one operating mode, locates a segment descriptor in a segment descriptor table in memory" as recited in claim 1.

For at least the above stated reasons, Applicant submits that claim 1 is patentable over Motorola and Motorola in view of Uffenbeck. Claims 2-9, being dependent from claim 1, are similarly patentable over Motorola and Motorola in view of Uffenbeck for at least the above stated reasons. Each of claims 2-9 recites additional combinations of features not taught or suggested in Motorola nor Motorola in view of Uffenbeck.

Claim 10 recites a combination of features including: "a first storage location corresponding to a segment register, the first storage location configured to store a segment base address and a selector which, in at least one operating mode, locates a segment descriptor in a segment descriptor table in memory...wherein the processor is configured, in response to a first instruction, to swap the segment base address in the first storage location and the address in the second storage location". The teachings of Motorola highlighted above with regard to claim 1 are also asserted to teach the above features of claim 10. Applicant respectfully submits that the teachings of Motorola do not teach or suggest the above highlighted features of claim 10, either. Accordingly, Applicant respectfully submits that claim 10 is patentable over Motorola and Motorola in view of Uffenbeck. Claims 11-17, being dependent from claim 10, are similarly patentable over Motorola and Motorola in view of Uffenbeck for at least the above stated

reasons. Each of claims 11-17 recites additional combinations of features not taught or suggested in Motorola nor Motorola in view of Uffenbeck.

Claim 18 recites a combination of features including: "A computer accessible storage medium storing an instruction which, when executed in a processor, causes a segment base address from a segment register and an address stored in a different register to be swapped, wherein the segment register is further configured to store a selector which, in at least one operating mode of the processor, locates a segment descriptor in a segment descriptor table in memory." The teachings of Motorola highlighted above with regard to claim 1 are also asserted to teach the above features of claim 18. Applicant respectfully submits that the teachings of Motorola do not teach or suggest the above highlighted features of claim 18, either. Additionally, the Office Action asserts that the "carrier medium" of claim 18 is taught by the sheet of paper on which the instruction is printed. Applicant respectfully submits that the sheet of paper does not teach or suggest a computer accessible storage medium as now recited in claim 18. Accordingly, Applicant respectfully submits that claim 18 is patentable over Motorola and Motorola in view of Uffenbeck. Claims 19-22, being dependent from claim 18, are similarly patentable over Motorola and Motorola in view of Uffenbeck for at least the above stated reasons. Each of claims 19-22 recites additional combinations of features not taught or suggested in Motorola nor Motorola in view of Uffenbeck.

Claim 23 recites a combination of features including: " A computer accessible storage medium storing an operating system routine including a first instruction which, when executed in a processor, causes a segment base address from a segment register and a base address stored in a register to be swapped, ... wherein the segment register is further configured to store a selector which, in at least one operating mode of the processor, locates a segment descriptor in a segment descriptor table in memory." The teachings of Motorola highlighted above with regard to claim 1 are also asserted to teach the above features of claim 23. Applicant respectfully submits that the teachings of Motorola do not teach or suggest the above highlighted features of claim 23, either. Additionally, the Office Action asserts that the "carrier medium" of claim 23 is taught by

the sheet of paper on which the instruction is printed. Applicant respectfully submits that the sheet of paper does not teach or suggest a computer accessible storage medium as now recited in claim 23. Accordingly, Applicant respectfully submits that claim 23 is patentable over Motorola and Motorola in view of Uffenbeck. Claims 24-29, being dependent from claim 23, are similarly patentable over Motorola and Motorola in view of Uffenbeck for at least the above stated reasons. Each of claims 24-29 recites additional combinations of features not taught or suggested in Motorola nor Motorola in view of Uffenbeck.

Sites Rejection

Applicant respectfully submits that each of claims 1-29 recites a combination of features not taught or suggested in Sites. For example, claim 1 recites a combination of features including: "a segment register configured to store a segment base address and a selector which, in at least one operating mode, locates a segment descriptor in a segment descriptor table in memory...wherein the execution core is configured, in response to a first instruction, to swap the segment base address in the segment register and the address in the register".

The present Office Action asserts that Sites teaches a segment register as the IKSP register. The IKSP register is described on page 2-4 as the initial kernel stack pointer. "The IKSP register contains the initial kernel stack address. The IKSP points to the top of the kernel stack for the currently executing thread." (Sites, page 2-4). Thus, it appears that Sites' IKSP register stores only a stack address. Sites' IKSP register does not teach or suggest "a segment register configured to store a segment base address and a selector which, in at least one operating mode, locates a segment descriptor in a segment descriptor table in memory" as recited in claim 1.

Furthermore, the Office Action asserts that Sites teaches the first instruction via the swpksp instruction described on page 5-33. However, the swpksp instruction swaps the IKSP register and another register (see Sites, page 5-33). This does not teach or suggest "the execution core is configured, in response to a first instruction, to swap the

segment base address in the segment register and the address in the register" wherein the segment register is "configured to store a segment base address and a selector which, in at least one operating mode, locates a segment descriptor in a segment descriptor table in memory" as recited in claim 1.

For at least the above stated reasons, Applicant submits that claim 1 is patentable over Sites. Claims 2-9, being dependent from claim 1, are similarly patentable over Sites for at least the above stated reasons. Each of claims 2-9 recites additional combinations of features not taught or suggested in Sites.

Claim 10 recites a combination of features including: "a first storage location corresponding to a segment register, the first storage location configured to store a segment base address and a selector which, in at least one operating mode, locates a segment descriptor in a segment descriptor table in memory...wherein the processor is configured, in response to a first instruction, to swap the segment base address in the first storage location and the address in the second storage location". The teachings of Sites highlighted above with regard to claim 1 are also asserted to teach the above features of claim 10. Applicant respectfully submits that the teachings of Sites do not teach or suggest the above highlighted features of claim 10, either. Accordingly, Applicant respectfully submits that claim 10 is patentable over Sites. Claims 11-17, being dependent from claim 10, are similarly patentable over Sites for at least the above stated reasons. Each of claims 11-17 recites additional combinations of features not taught or suggested in Sites.

Claim 18 recites a combination of features including: "A computer accessible storage medium storing an instruction which, when executed in a processor, causes a segment base address from a segment register and an address stored in a different register to be swapped, wherein the segment register is further configured to store a selector which, in at least one operating mode of the processor, locates a segment descriptor in a segment descriptor table in memory." The teachings of Sites highlighted above with regard to claim 1 are also asserted to teach the above features of claim 18. Applicant

respectfully submits that the teachings of Sites do not teach or suggest the above highlighted features of claim 18, either. Additionally, the Office Action asserts that the "carrier medium" of claim 18 is taught by the sheet of paper on which Sites is printed. Applicant respectfully submits that the sheet of paper does not teach or suggest a computer accessible storage medium as now recited in claim 18. Accordingly, Applicant respectfully submits that claim 18 is patentable over Sites. Claims 19-22, being dependent from claim 18, are similarly patentable over Sites for at least the above stated reasons. Each of claims 19-22 recites additional combinations of features not taught or suggested in Sites.

Claim 23 recites a combination of features including: "A computer accessible storage medium storing an operating system routine including a first instruction which, when executed in a processor, causes a segment base address from a segment register and a base address stored in a register to be swapped, ... wherein the segment register is further configured to store a selector which, in at least one operating mode of the processor, locates a segment descriptor in a segment descriptor table in memory." The teachings of Sites highlighted above with regard to claim 1 are also asserted to teach the above features of claim 23. Applicant respectfully submits that the teachings of Sites do not teach or suggest the above highlighted features of claim 23, either. Additionally, the Office Action asserts that the "carrier medium" of claim 23 is taught by the sheet of paper on which Sites is printed. Applicant respectfully submits that the sheet of paper does not teach or suggest a computer accessible storage medium as now recited in claim 23. Accordingly, Applicant respectfully submits that claim 23 is patentable over Sites. Claims 24-29, being dependent from claim 23, are similarly patentable over Sites for at least the above stated reasons. Each of claims 24-29 recites additional combinations of features not taught or suggested in Sites.

Hubicka Rejection

The rejection of claims 18-29 over Hubicka alleges that Hubicka anticipates the claims because Hubicka's piece of paper corresponds to the carrier medium. Claims 18-29 now recite a computer accessible storage medium. Applicant respectfully submits that

Hubicka's piece of paper does not teach or suggest a computer accessible storage medium.

Furthermore, Applicant notes that Hubicka does not describe anything about how the swapgs instruction works. Thus, Hubicka does not teach "A computer accessible storage medium storing an instruction which, when executed in a processor, causes a segment base address from a segment register and an address stored in a different register to be swapped, wherein the segment register is further configured to store a selector which, in at least one operating mode of the processor, locates a segment descriptor in a segment descriptor table in memory" as recited in claim 18 nor "A computer accessible storage medium storing an operating system routine including a first instruction which, when executed in a processor, causes a segment base address from a segment register and a base address stored in a register to be swapped, ... wherein the segment register is further configured to store a selector which, in at least one operating mode of the processor, locates a segment descriptor in a segment descriptor table in memory" as recited in claim 23.

For at least the above stated reasons, Applicant respectfully submits that claims 18 and 23 are patentable over Hubicka. Claims 19-22, being dependent from claim 18, and claim 24-29, being dependent from claim 23, are similarly patentable over Hubicka for at least the above stated reasons. Each of claims 19-22 and 24-29 recites additional combinations of features not taught or suggested in Hubicka.

Section 101 Rejection

Claims 18-29 were rejected under 35 U.S.C. § 101 as being nonstatutory, because the term "carrier medium" may include electronic signals. Applicant has amended claims 18-29 to recite a "computer accessible storage medium" that stores various instructions. Applicant respectfully submits that a computer accessible storage medium is statutory.

Section 112 Rejection

Claims 10-17 were rejected under 35 U.S.C. § 112, second paragraph because

claim 10, in the last clause, included the phrase "and the and the". Applicant has amended claim 10 to strike the second occurrence of "and the", and submit that the amendment addresses the rejection.

New Claims

Applicant respectfully submits that new claims 31-35 each recite a combination of features not taught or suggested in the cited art. For example, claim 31 recites a combination of features including: "A computer accessible storage medium storing a plurality of instructions which, when executed in a processor responsive to a first instruction, cause a segment base address from a storage location corresponding to a segment register and an address stored in a different storage location corresponding to a different register to be swapped, wherein the storage location corresponding to the segment register is further configured to store a selector which, in at least one operating mode of the processor, locates a segment descriptor in a segment descriptor table in memory." Claims 32-35 depend from claim 31 and recite additional combinations of features not taught or suggested in the cited art.

Title Objection

The Office Action objected to the title as being imprecise. Applicant has amended the title, and respectfully submits that the amended title addresses the objection.

PTO-1449 Form

Applicant received the PTO-1449 form from the Information Disclosure Statement filed November 15, 2001. The Examiner signed the form, and initialed the non-patent references. However, two patent references were also listed on the PTO-1449 form, and these references were not initialed. As the references were also not crossed out on the PTO-1449 form, Applicant believes that the missing initials are merely an oversight. Applicant has attached hereto a copy of the returned PTO-1449 form with the missing initials highlighted. Applicant respectfully requests that the Examiner initial the patent references to evidence consideration thereof, and return the form with the next Action.

CONCLUSION

Applicant submits that the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-78100/LJM.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Petition for Extension of Time

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

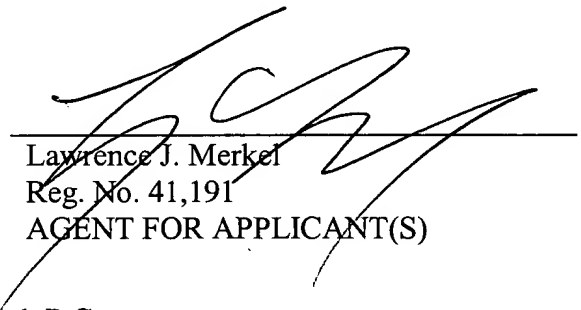
☐ Marked-up Copy of Amended Claims

☐ Marked-up Copy of Amended Paragraphs

☒ Please debit the above deposit account in the amount of $72 for fees ($72 for four excess claims over 20).

☒ Other: Previously Returned PTO-1449 form with missing initials highlighted

Respectfully submitted,



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Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5500-78100 APPLICANT: McGrath FILING DATE: August 9, 2001	SERIAL NO. 09/927,054 GROUP: 2183

U.S. PATENT DOCUMENTS							
	A9	5,684,993	11/4/97	Willman			
	A18	5,418,956	5/23/95	Willman			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
RLE	A1	The Technology Behind Crusoe™ Processors, Low-Power x86-Compatible Processors Implemented with Code Morphing™ Software, Transmeta Corporation, January 2000, pages 1-18.
RLE	A2	Alpha Learns to Do Windows; Digital's FX!32 is The Key To Running Win32 Software on Alpha/Windows NT., Selinda Chiquoine, BYTE, August 4, 1998, 4 pages.
RLE	A3	Awards Stack Up for DIGITAL FX!32 Windows Compatibility Software for ALPHA, DIGITAL Press Releases, December 11,1 997, 7 pages.
RLE	A4	DIGITAL FX!32; White Paper: How DIGITAL FX!32 Works, DIGITAL Semiconductor, January 26, 1998, 4 pages.
RLE	A5	An Alpha in PC Clothing; Digital Equipment's New x86 Emulator Technology Makes An Alpha System a Fast x86 Clone, Tom Thompson, BYTE, August 4, 1998, 7 pages.
RLE	A6	AMD 64-Bit Technology; The AMD x86 Architecture Programmers Overview, AMD, Publication #24108 Rev: A, August 2000, pages 1-106.
RLE	A7	AMD 64-Bit Technology; The AMD x86-64 Architecture Programmers Overview, AMD, Publication #24108 Rev: C, January 2001, pages 1-128.
RLE	A8	Alpha Architecture Reference Manual, Third Edition, Digital Press, 1998 Digital Equipment Corporation, pages 5-14 to 5-15, 5-18 to 5-19, 5-30 to 5-35.
RLE	A10	32-Bit Microprocessor User's Manual, MC68020, Third Edition, Motorola, 1989, pp. 3-105 and 3-184..
RLE	A11	Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, 1997, pages 6-17 to 6-19.
RLE	A12	Intel, "Intel Architecture Software Developer's Manual, Vol. 2: Instruction Set Reference," 1997, pages 3-29, 3-66 to 3-69, 3-196 to 3-197, 3-460 to 3-463..
RLE	A13	AMD, "SYSCALL and SYSRET Instruction Specification", Application Note, 1998, pages 1-10.
RLE	A14	Intel, "Intel Architecture Software Developer's Manual, Vol. 2: Instruction Set Reference," 1997, pages 3-256 to 3-258, 3-286 to 3-290, 3-350 to 3-353, 3-385 to 3-387.
RLE	A15	Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture, 1997, pages 3-38 to 3-39.
RLE	A16	Addendum-Intel Architecture Software Developer's Manual, Vol. 2: Instruction Set Reference, 1996/1997, Chapter 3, pages 3-1 to 3-15.
RLE	A17	Pentium Pro Family Developer's Manual, Volume 3: Operating System Writer's Guide, 1996, pages 2-1 to 2-21, 3-1 to 3-33, 4-1 to 4-29.

EXAMINER: Richard Ellis DATE CONSIDERED: 9/23/2004

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.